CLAIM AMENDMENTS

1. (original) An on-chip inductor consisting of:

at least one dielectric layer;

at least one conductive winding on the at least one dielectric layer; and

P-well having a major surface parallel to a major surface of the dielectric layer.

2. (original) The on-chip inductor of claim 1 further consists of:

a field oxide having a major surface that is juxtaposed to the major surface of the P-well.

3. (original) The on-chip inductor of claim 1 further consists of:

the at least one dielectric layer including one layer; and

the at least one conductive winding including a spiral winding on the one layer.

4. (original) The on-chip inductor of claim 1 further consists of:

the at least one dielectric layer includes a plurality of layers; and

the at least conductive winding includes a plurality of windings on the plurality of layers.

5. (withdrawn) The on-chip inductor of claim 1 further consists of:

the at least one dielectric layer includes a plurality of layers; and

the at least conductive winding includes a plurality of spiral windings on the plurality of layers.

6. (original) The on-chip inductor of claim 1 further consists of:

a substrate having a major surface parallel to the major surface of the at least one dielectric layer.

7. (original) The on-chip inductor of claim 1 further consists of:

a secondary winding magnetically coupled to the conductive winding.

8. (withdrawn) The on-chip inductor of claim 1, wherein the at least one conductive winding further consists of:

center tap operably coupled to a reference potential to produce a differential inductor.

9. (original) An on-chip inductor consisting of:

at least one dielectric layer;

at least one conductive winding on the at least one dielectric layer; and

field oxide layer having a major surface parallel to a major surface of the dielectric layer.

10. (original) The on-chip inductor of claim 9 further consists of:

P-well having a major surface that is juxtaposed to the major surface of the field oxide layer.

11. (original) The on-chip inductor of claim 9 further consists of:

a secondary winding magnetically coupled to the conductive winding.

12. (withdrawn) The on-chip inductor of claim 9, wherein the at least one conductive winding further consists of:

center tap operably coupled to a reference potential to produce a differential inductor.

13. (withdrawn) An on-chip inductor consisting of:

at least one dielectric layer;

at least one conductive winding on the at least one dielectric layer; and

poly silicon layer having a major surface parallel to a major surface of the dielectric layer.

14. (withdrawn) The on-chip inductor of claim 13 further consists of:

a secondary winding magnetically coupled to the conductive winding.

15. (withdrawn) The on-chip inductor of claim 13, wherein the at least one conductive winding further consists of:

center tap operably coupled to a reference potential to produce a differential inductor.